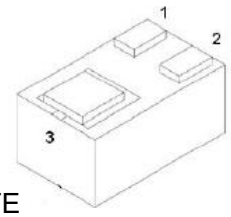
$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
20V	380 m Ω@4.5V	0.75A
	450m Ω@2.5V	
	800 mΩ@1.8V	

WBFBP-03E



1.GATE
2.SOURCE
3.DRAIN

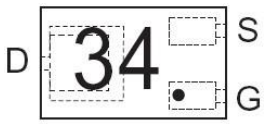
FEATURE

- Lead Free Product is Acquired
- Surface Mount Package
- N-Channel Switch with Low R_{DS}(on)
- Operated at Low Logic Level Gate Drive
- ESD Protected Gate
- Complementary to CJAA3139K

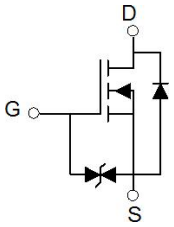
APPLICATION

- Load/ Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

MARKING:



Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Typical Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (note 1)	I_D	0.75	A
Pulsed Drain Current (tp=10us)	I_{DM}	1.8	A
Power Dissipation (note 1)	P_D	100	mW
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	1250	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ 150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

MOSFET ELECTRICAL CHARACTERISTICS

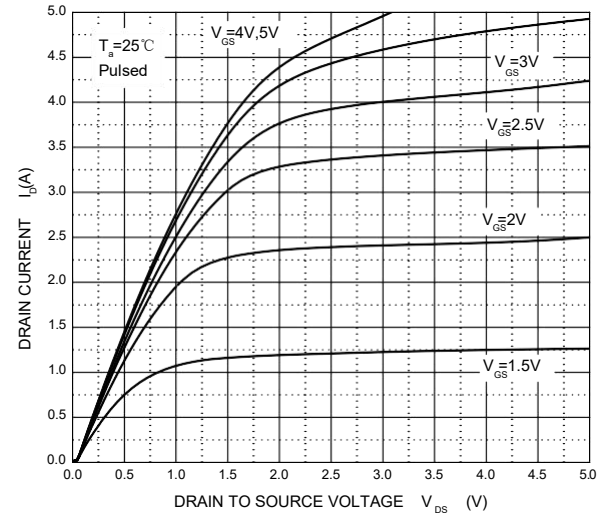
T_a=25 ℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±10V, V_{DS} = 0V			±20	uA
Gate threshold voltage (note 2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.35		1.1	V
Drain-source on-resistance(note 2)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =0.65A			380	mΩ
		V_{GS} =2.5V, I_D =0.55A			450	mΩ
		V_{GS} =1.8V, I_D =0.45A			800	mΩ
Forward tranconductance(note 2)	g_{FS}	V_{DS} =10V, I_D =0.8A		1.6		S
Diode forward voltage	V_{SD}	I_S=0.15A, V_{GS} = 0V			1.2	V
DYNAMIC PARAMETERS(note 4)						
Input Capacitance	C_{iss}	V_{DS} =16V,V_{GS} =0V,f =1MHz		79	120	pF
Output Capacitance	C_{oss}			13	20	pF
Reverse Transfer Capacitance	C_{rss}			9	15	pF
SWITCHING PARAMETERS (note 4)						
Turn-on delay time (note 3)	$t_{d(on)}$	V_{DD}=4.5V,V_{GS}=10V, I_D=500mA,R_{GEN}=10Ω		6.7		ns
Turn-on rise time (note 3)	t_r			4.8		ns
Turn-off delay time (note 3)	$t_{d(off)}$			17.3		ns
Turn-off fall time (note 3)	t_f			7.4		ns

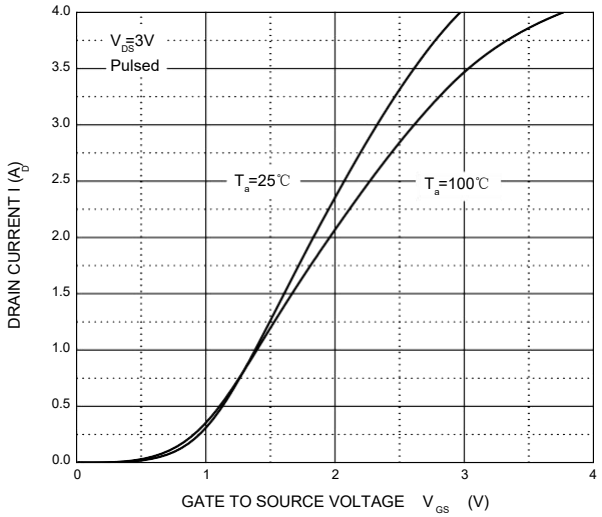
Notes :

1. Surface mounted on FR4 board using the minimum recommended pad size.
2. Pulse Test : Pulse width=300μs, duty cycle≤2%.
3. Switching characteristics are independent of operating junction temperatures.
4. Graranted by design，not subject to producting.

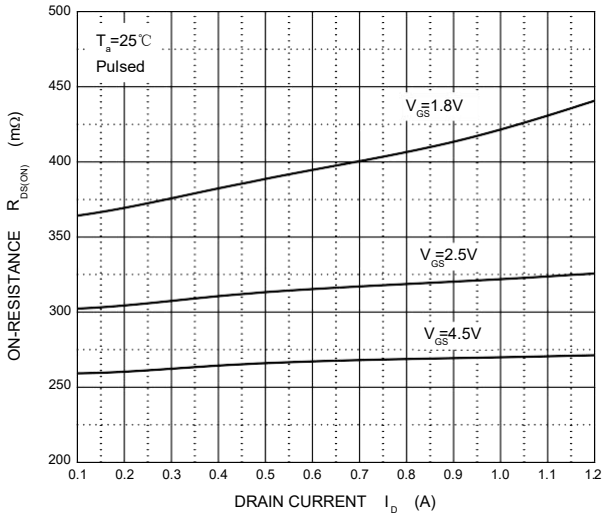
Output Characteristics



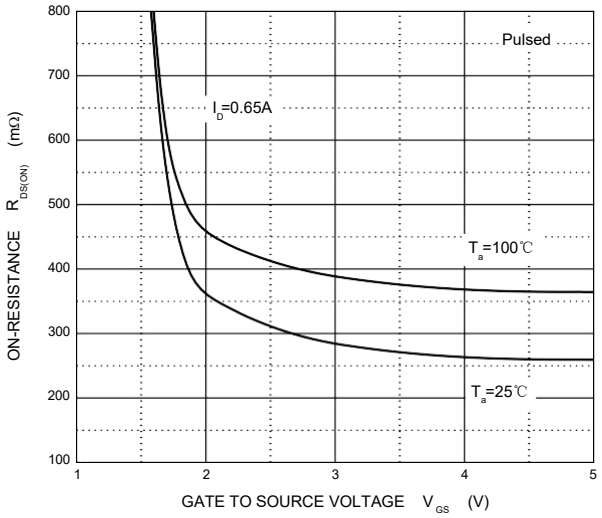
Transfer Characteristics



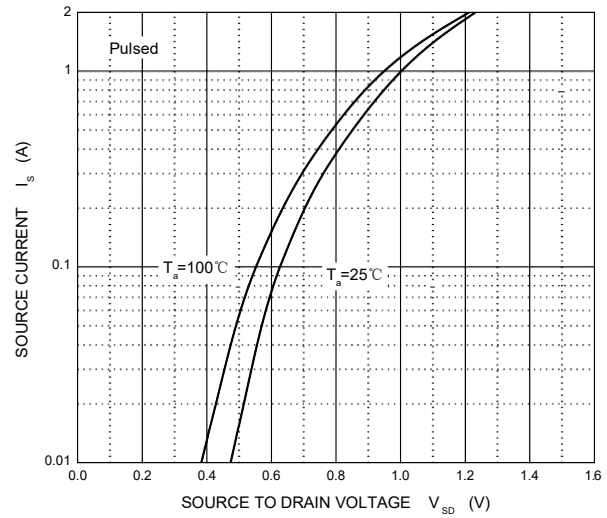
$R_{DS(ON)}$ —— I_D



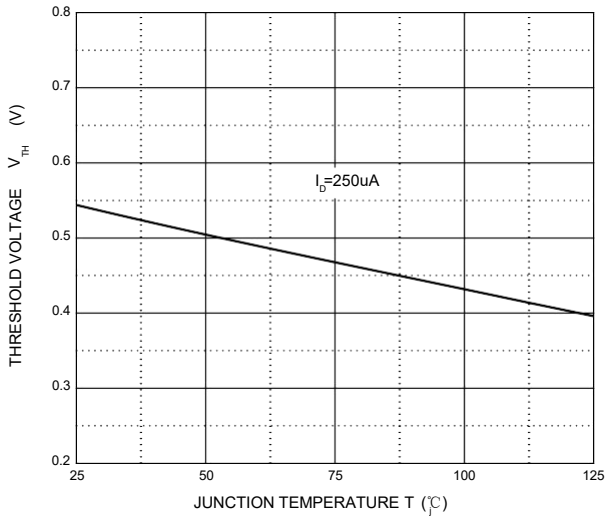
$R_{DS(ON)}$ —— V_{GS}



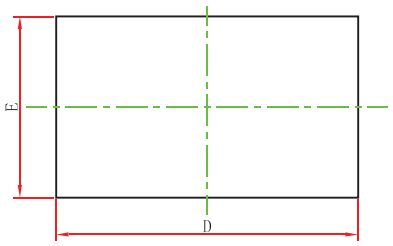
I_S —— V_{SD}



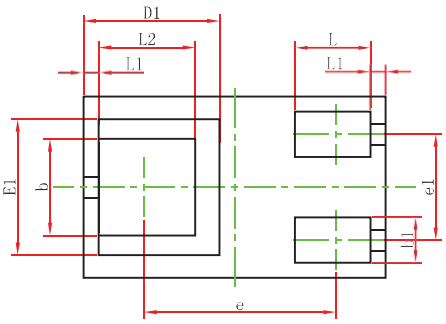
Threshold Voltage



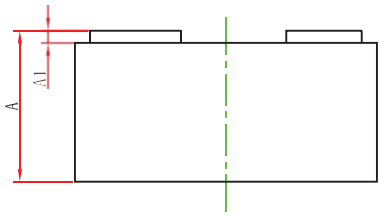
WBFBP-03E Package Outline Dimensions



TOP VIEW



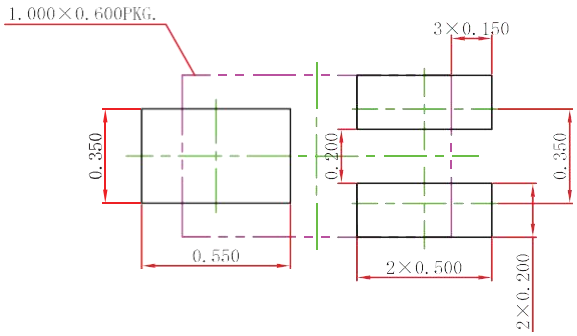
BOTTOM VIEW



SIDE VIEW

6\PERO	'LPHQVLRQV ,Q 0LOOLPHWHUV		'LPHQVLRQV ,Q ,QFKHV	
	0LQ.	0D[.	0LQ.	0D[.
$	0.4±0	0.±±0	0.018	0.0²²
$1	0.010	0.100	0.000	0.004
'	0.9±0	1.0±0	0.03F	0.041
(	0.±±0	0.6±0	0.0²²	0.0²6
'1	0.4±05().		0.0185().	
(1	0.4±05().		0.0185().	
E	0.²F0	0.3F0	0.011	0.01±
E1	0.100	0.²00	0.004	0.008
H	0.63±5().		0.0²±5().	
H1	0.300	0.400	0.01²	0.016
/	0.²00	0.300	0.008	0.01²
/1	0.0±05().		0.00²5().	
/²	0.²F0	0.3F0	0.011	0.01±

WBFBP-03E Suggested Pad Layout



Note:

1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.