# ESD Protection Diodes with Ultra−Low Capacitance

The ESDBL7V0AE1 is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

DFN0603-D


**Specification Features:**

- Ultra Low Capacitance 3 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
  (0.61 mm x 0.31 mm)
- Low Body Height: 0.28 mm
- Stand−off Voltage: 7 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- This is a Pb−Free Device

**Mechanical Characteristics:**

**CASE:** Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V−0
**LEAD FINISH:** 100% Matte Sn (Tin)

**MAXIMUM RATINGS**

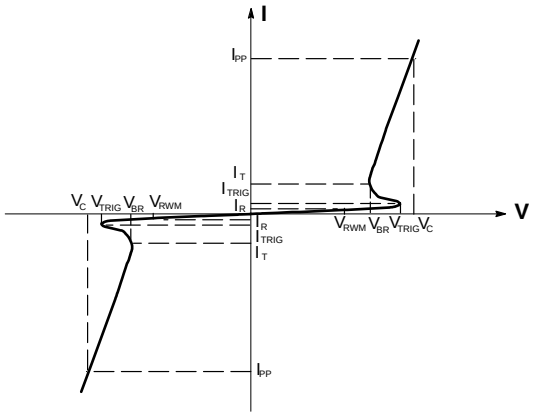
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| IEC 61000−4−2 (ESD) Contact<br>Air | | ±10<br>±15 | kV |
| Total Power Dissipation on FR−5 Board (Note 1) @ $T_A$ = 25°C | $P_D$ | 200 | mW |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Junction Temperature Range | $T_J$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Second Duration) | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.62 in.

## ELECTRICAL CHARACTERISTICS
($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Reverse standoff voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $V_{TRIG}$ | Reverse trigger voltage |
| $I_{TRIG}$ | Reverse trigger current |




**Bi−Directional TVS**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Device | Device Marking | $V_{RWM}$ (V) | $I_R$ (uA) @ $V_{RWM}$ | $V_{BR}$ (V) @ $I_T$ = 1mA (Note 2) | | C (pF) | | $V_C$ (V) @ $I_{PP}$ = 3.5 A (Note 3) | $I_{PP}$ (A) $t_p$=8/20μs | $P_{PP}$ (W) | $V_C$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max | Max | Min | Max | Typ | Max | Max | Max | Max | Per IEC61000−4−2 (Note4) |
| ESDBL7V0AE1 | C | 7.0 | 1 | 5.5 | 9.6 | 2.7 | 3.5 | 11.5 | 3.5 | 40 | Figures 1 and 2 See Below |

2. $V_{BR}$ is measured with a pulse test current $I_T$ at an ambient temperature of 25°C.
3. Surge current waveform per Figure 4.
4. For test procedure see Figures 3.

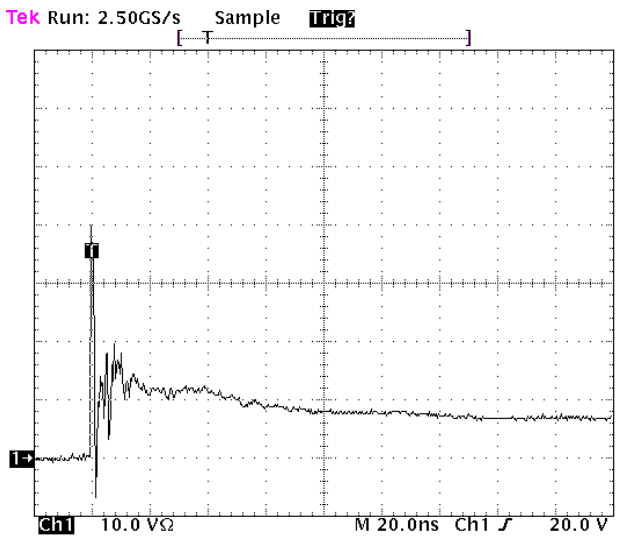



**Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2**

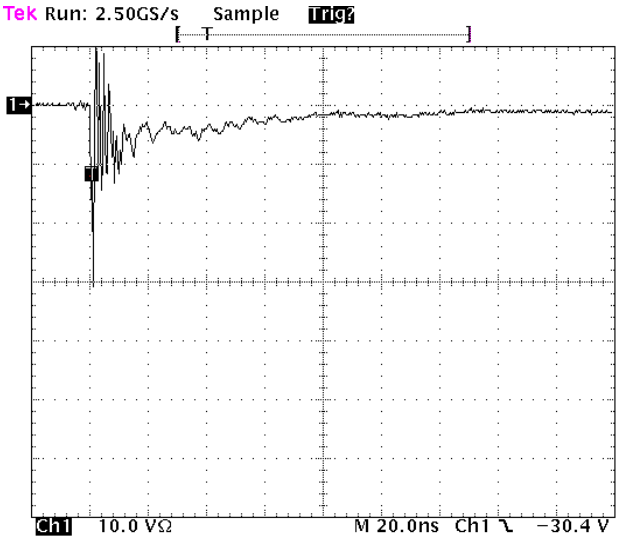



**Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2**

**IEC 61000–4–2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

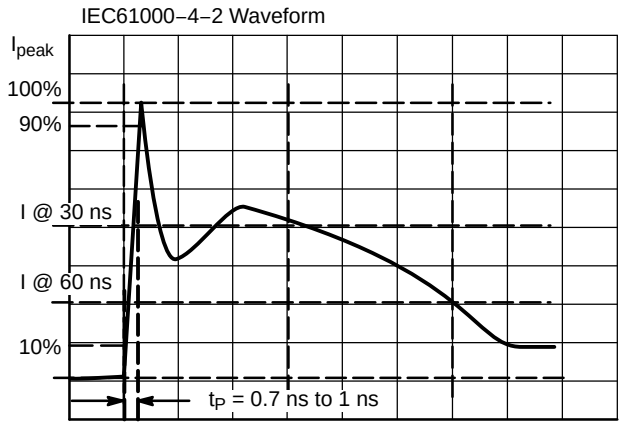



**Figure 3. IEC61000–4–2 Spec**

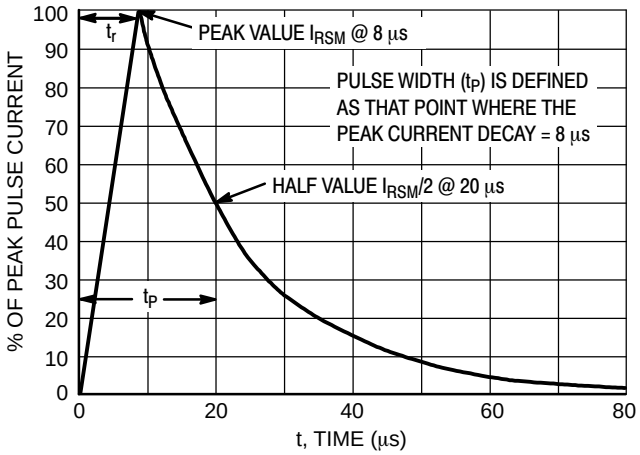
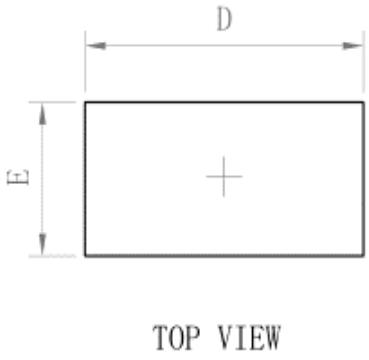
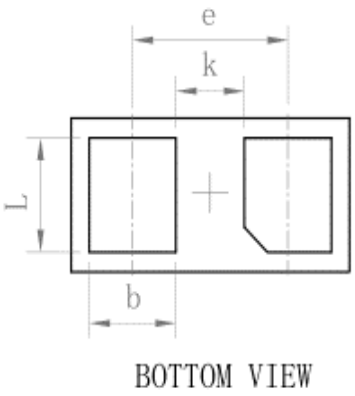



**Figure 4. 8 X 20 μs Pulse Waveform**

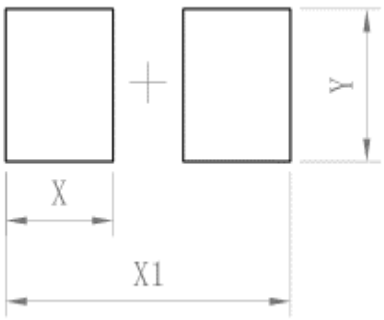
**OUTLINE AND DIMENSIONS**




| DFN0603-D | | | |
|---|---|---|---|
| Dim | Min | Typ | Max |
| D | 0.56 | 0.61 | 0.66 |
| E | 0.26 | 0.31 | 0.36 |
| e | - | 0.34 | - |
| L | 0.18 | 0.23 | 0.28 |
| b | 0.14 | 0.19 | 0.24 |
| A | 0.23 | 0.28 | 0.33 |
| k | 0.10 | 0.15 | 0.20 |
| All Dimensions in mm | | | |


**SOLDERING FOOTPRINT**




| Dimensions | (mm) |
|---|---|
| X | 0.23 |
| X1 | 0.61 |
| Y | 0.30 |